



IPW

Serial No. 10/615,003

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Greg A. Blodgett

Examiner: Unknown

Serial No.: 10/615,003

Group Art Unit: Unknown

Filed: July 8, 2003

Docket: 303.128US3

Title: CONTINUOUS INTERLEAVE BURST ACCESS

COMMUNICATION CONCERNING RELATED APPLICATIONS

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant would like to bring to the Examiner's attention the following related applications in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
08/661478 5802010	June 11, 1996	303.228US1	BURST EDO MEMORY DEVICE
08/984701	December 3, 1997	303.623US5	BURST/PIPELINED EDO MEMORY DEVICE WITH MODE SELECT PIN
08/984561 6615325	December 3, 1997	303.623US6	METHOD FOR SWITCHING BETWEEN MODES OF OPERATION
08/553156 5721859	November 7, 1995	303.058US1	COUNTER CONTROL CIRCUIT IN A BURST MEMORY
08/552199 5668773	November 2, 1995	303.059US1	SYNCHRONOUS BURST EXTENDED DATA OUT DRAM
08/811696 5812488	March 5, 1997	303.059US2	SYNCHRONOUS BURST EXTENDED DATA OUT DRAM
08/553986 5682354	November 6, 1995	303.060US1	CAS RECOGNITION IN BURST EXTENDED DATA OUT DRAM
08/890418 5831931	July 9, 1997	303.060US2	ADDRESS STROBE RECOGNITION IN A MEMORY DEVICE

08/568358 5640364	December 6, 1995	303.061US1	SELF-ENABLING PULSE-TRAPPING CIRCUIT
08/914659 5831932	August 19, 1997	303.061US3	SELF-ENABLING PULSE-TRAPPING CIRCUIT
08/572487 5729504	December 14, 1995	303.062US1	CONTINUOUS BURST EDO MEMORY DEVICE
08/891557 5946265	July 11, 1997	303.062US2	CONTINUOUS OUTPUT MEMORY DEVICE
08/370761 5526320	December 23, 1994	303.100US1	BURST EDO MEMORY DEVICE
08/630279 5661695	April 11, 1996	303.100US2	BURST EDO MEMORY DEVICE
08/754780 5696732	November 21, 1996	303.100US3	BURST EDO MEMORY DEVICE
08/675139 6401186	July 3, 1996	303.128US1	CONTINUOUS BURST MEMORY WHICH ANTICIPATES A NEXT REQUESTED START ADDRESS
10/118299 6601156	April 8, 2002	303.128US2	CONTINUOUS INTERLEAVE BURST ACCESS
08/386894 5610864	February 10, 1995	303.161US1	BURST EDO MEMORY DEVICE WITH MAXIMIZED WRITE CYCLE TIMING
08/797339 5717654	February 10, 1997	303.161US2	BURST EDO MEMORY DEVICE WITH MAXIMIZED WRITE CYCLE TIMING
08/386563 5652724	February 10, 1995	303.162US1	BURST EDO MEMORY DEVICE HAVING PIPELINED OUTPUT BUFFER
08/457651 5675549	June 1, 1995	303.163US1	BURST EDO MEMORY ADDRESS COUNTER

COMMUNICATION CONCERNING RELATED APPLICATIONS

Serial Number: 10/615,003

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Title: CONTINUOUS INTERLEAVE BURST ACCESS

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Dkt: 303.128US3

08/922194 5850368	September 2, 1997	303.163US2	BURST EDO MEMORY ADDRESS COUNTER
08/497354 5598376	June 30, 1995	303.165US1	DISTRIBUTED WRITE DATA DRIVERS FOR BURST ACCESS MEMORIES
08/785867 5757703	January 21, 1997	303.165US2	DISTRIBUTED WRITE DATA DRIVERS FOR BURST ACCESS MEMORIES
09/361795 6525971	July 27, 1999	303.165US4	DISTRIBUTED WRITE DATA DRIVERS FOR BURST ACCESS MEMORIES
08/505576	July 21, 1995	303.166US1	MAIN MEMORY SYSTEM WITH MULTIPLE DATA PATHS FOR HIGH PERFORMANCE AND HIGH CAPACITY
08/506438 5729503	July 24, 1995	303.167US1	ADDRESS TRANSITION DETECTION IN A SYNCHRONOUS DESIGN
08/994180 5963504	December 19, 1997	303.167US2	ADDRESS TRANSITION DETECTION IN A SYNCHRONOUS DESIGN
08/584600 5966724	January 11, 1996	303.169US1	SYNCHRONOUS MEMORY DEVICE WITH DUAL PAGE AND BURST MODE OPERATIONS

10/231682	August 29, 2002	303.165US5	DISTRIBUTED WRITE DATA DRIVERS FOR BURST ACCESS MEMORIES
10/232978	August 29, 2002	303.165US7	DISTRIBUTED WRITE DATA DRIVERS FOR BURST ACCESS MEMORIES

Respectfully submitted,

GREG A. BLODGETT

By Applicant's Representatives,

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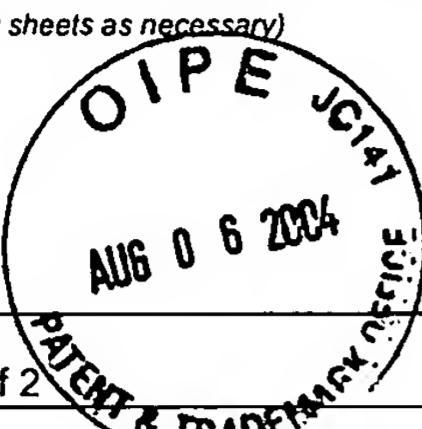
Date 8-4-04

By Marvin L. Beekman
Marvin L. Beekman
Reg. No. 38,377

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JAMES KANYUSIK
Name

James Kanyusik
Signature

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Complete if Known Application Number 10/615,003 Filing Date July 8, 2003 First Named Inventor Blodgett, Greg Group Art Unit Unknown Examiner Name Unknown				
Sheet 1 of 2 		Attorney Docket No: 303.128US3				

US PATENT DOCUMENTS						
Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-4,195,770	04/01/1980	Benton, Michael K., et al.	371	21.2	10/24/1978
	US-4,594,587	06/10/1986	Chandler, Gregg , et al.	340	750	08/30/1983
	US-4,857,899	08/15/1989	Ishii, Takatoshi	340	701	12/10/1986
	US-5,243,699	09/07/1993	Nickolls, John R., et al.	395	275	12/06/1991
	US-5,568,651	10/22/1996	Medina, Eitan , et al.	395	894	11/03/1994
	US-5,587,950	12/24/1996	Sawada, Seiji , et al.	365	201	06/05/1995
	US-5,594,704	01/14/1997	Konishi, Yasuhiro , et al.	365	233	04/10/1995

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS		
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
		"Chips: Intel Corp. intros higher performing PCI chip set for Pentium processors; Triton architecture unlocks Pentium processor power necessary for multitude of applications (Intel Corp.'s 82430FX)", <u>EDGE: Work-Group Computing Report</u> , vol. 6, no. 246, (1995),10(1)
		"Intel Readies Triton PCI chipset (Intel's 82430FX)", <u>Electronic News</u> , Vol. 41, No. 2050, (1995),68(1)
		GOWNI, SHIVA P., et al., "A 9NS, 32K X 9, BiCMOS TTL Synchronous Cache RAM with Burst ;Mode Access", <u>IEEE 1992 Custom Integrated Circuits Conference</u> , Boston USA,(May 1992),7.8.1-7.8.4
		INTEL, "Intel Electronic News", <u>ISSN: 1061-6624</u> , <u>Electronic News Publishing Corp.</u> , (12-05-94),26
		INTEL CORPORATION, "82430FX PCIset DATASHEET 82437FX SYSTEM CONTROLLER (TSC) AND 82438FX DATA PATH UNIT (TDP)", <u>Intel Corporation</u> , Order No. 290518-002,(November 1996),1-67
		JENISCH, E. , et al., "P55TP4 (Triton-based)-SYNC/BURST SRAMS?", <u>www.google.com</u> , (1995),7 pages
		MICRON, "DRAM 1 Meg X 4 DRAM 5VEDO Page Mode", <u>Micron Technology, Inc.</u> DRAM Data Book, (1995),1-1 thru 1-30
		MICRON SEMICONDUCTOR INC., ""Synchronous DRAM 2 MEG X 8 SDRAM"" , (Rev. 4/94)),2-43 through 2-83
		MOSEL-VITELIC, "Mosel-Vitelic V53C8257H DRAM Specification Sheet", (July 2, 1994),20 pgs.
		SAMSUNG ELECTRONICS, "Samsung Synchronous DRAM", (March 1993),1-16

EXAMINER

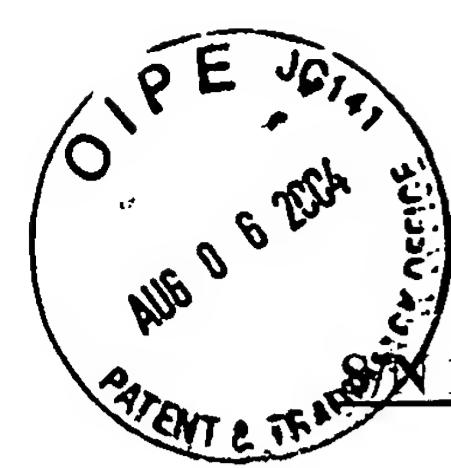
DATE CONSIDERED

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		<i>Complete if Known</i> <table border="1"> <tr> <td>Application Number</td> <td>10/615,003</td> </tr> <tr> <td>Filing Date</td> <td>July 8, 2003</td> </tr> <tr> <td>First Named Inventor</td> <td>Blodgett, Greg</td> </tr> <tr> <td>Group Art Unit</td> <td>Unknown</td> </tr> <tr> <td>Examiner Name</td> <td>Unknown</td> </tr> </table>		Application Number	10/615,003	Filing Date	July 8, 2003	First Named Inventor	Blodgett, Greg	Group Art Unit	Unknown	Examiner Name	Unknown
Application Number	10/615,003												
Filing Date	July 8, 2003												
First Named Inventor	Blodgett, Greg												
Group Art Unit	Unknown												
Examiner Name	Unknown												
Sheet 2 of 2		Attorney Docket No: 303.128US3											

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		SIMCHECK, "Old SIMCHECK Product Line", <u>Product Information, obtained from http://www.simcheck.com, (1995),1-3</u>	
		SULLIVAN, K. , "Slimcheck Add-on Lets Users Identify Faulty DRAM Chips", <u>PC Week, 7(18), (Obtained from Computer Select, Document No. 46161),(May 1990),18</u>	
		TATOSIAN, D. , "Detecting EDO RAM with Triton Mainboards", <u>http://www.deganews.com,(1995),2 pgs.</u>	
		TOSHIBA, "4M DRAM 1991", <u>Toshiba America Electronic Components, Inc., (1991),A-137 - A-159</u>	
		TOSHIBA, "Pipelined Burst DRAM", <u>Toshiba, JEDEC JC 42.3 Hawaii, (December 1994),9 pgs.</u>	

EXAMINER

DATE CONSIDERED



10/615,003

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Greg A. Blodgett	Examiner:	Unknown
Serial No.:	10/615,003	Group Art Unit:	Unknown
Filed:	July 08, 2003	Docket:	303.128US3
Title:	CONTINUOUS INTERLEAVE BURST ACCESS		

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicant with the next official communication.

Pursuant to 37 C.F.R. § 1.97(b), it is believed that no fee or statement is required with the Supplemental Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Supplemental Information Disclosure Statement considered.

The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

The present application is a U.S. national patent application filed after June 30, 2003. Thus, Applicant believes that the U.S. Patent & Trademark Office has waived the requirement under 37 C.F.R. 1.98 (a)(2)(i) for submitting a copy of each cited U.S. patent and each U.S. patent application publication. The waiver is provided in a pre-OG notice from the U.S. Patent & Trademark Office entitled "Information Disclosure Statements May Be Filed Without Copies of U.S. Patents and Published Applications in Patent Applications filed after June 30, 2003" and dated July 11, 2003. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

Respectfully submitted,

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By his Representatives,

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Date 8-4-04

By Marvin L. BEEKMAN
Marvin L. BEEKMAN
Reg. No. 38,377

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JAMES KAWYKLIK
Name

James Kawayklik
Signature



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Greg A. Blodgett
Title: CONTINUOUS INTERLEAVE BURST ACCESS

Docket No.: 303.128US3 Serial No.: 10/615,003
Filed: July 8, 2003 Due Date: N/A
Examiner: Unknown Group Art Unit: Unknown

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Commissioner for Patents
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We are transmitting herewith the following attached items (as indicated with an "X"):

- A return postcard.
 - A Communication Concerning Related Applications (4 pgs.).
 - A Supplemental Information Disclosure Statement (2 pgs.), Form 1449 (2 pgs.), and copies of 15 cited documents.

If not provided for in a separate paper filed herewith, Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
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By: Marvin L. Beekman
Atty: Marvin L. Beekman
Reg. No. 38,377

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JAMES KANYUSIK

day of August, 2004.



Signature

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
(GENERAL)